1. Introduction

Early versions of the latching ferrite phase shifters used discrete lengths of ferrite to provide phase quantization. Thus, a four-bit phase shifter consisted of cascading four sections of ferrite (of length *l, 2l, 4l, 8l*) separated by dielectric spacers which provided magnetic isolation. Each individual bit operated at the maximum remanent magnetization (plus or minus) so that a simple electronic circuit was adequate to control the phase shifter. However, machining and assembly of discrete ferrite sections is expensive. Furthermore, variations of remanent magnetization with temperature and frequency cannot be compensated easily with this type control. Most phase shifters are now constructed from a continuous section of ferrite with the phase shift quantization, frequency compensation and temperature compensation allocated to the electronic driver. The driver accomplishes these tasks by operating the ferrite in a partially magnetized state. As the magnetization varies from negative saturation to positive saturation, the relative permeability of the ferrite is controlled by adjusting the magnetic flux density in the ferrite core. The flux change cycle consists of a "reset" portion plus a "phase set" portion, as indicated by the sketches of Fig. 1. The purpose of the reset portion is to establish a reference limit-condition of magnetization of the ferrite. The phase-set portion of the cycle meters the change of flux away from this reference. It is important to establish the reference point in a repeatable manner, since the precision of phase setting is directly dependent on this condition. Phase shift is then accomplished by changing insertion phase from the reference point. The "memory" property of the ferrite material hysteresis loop is essential in allowing remanent-flux operation at a desired phase state, but tends to work against establishing a repeatable reset reference. Experience has shown that there is a tendency for the apparent reset phase state to wander in a manner dependent on the previous phase-set history of the unit. An improvement in the reset accuracy can be achieved by restricting all flux change operations to movements around the major hysteresis loop. Reset from a given remanent point is accomplished by first driving to the longest phase shift end of the hysteresis loop ("full set") and then driving to the opposite end of the loop
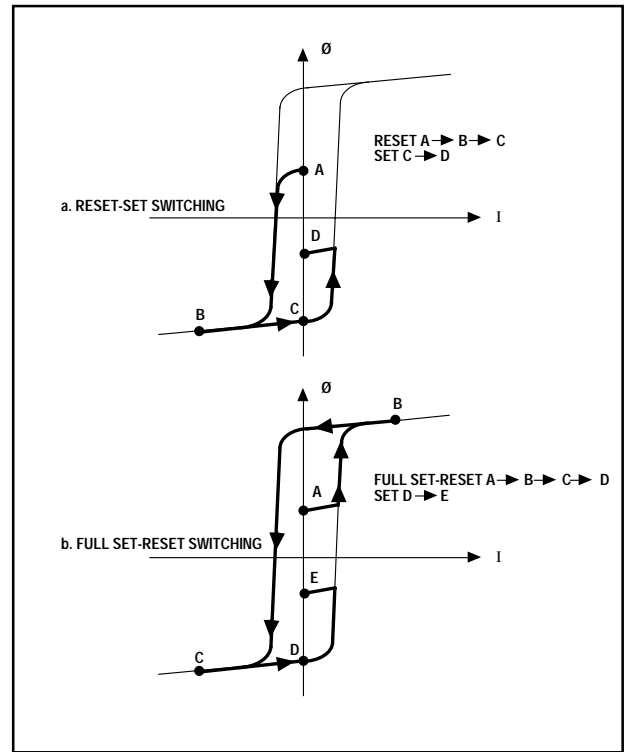

Figure 1. *Flux Change Cycles.*

("full reset"). Using this approach, adequate accuracy is possible with the peak current level as the criterion for terminating the full set and full reset pulses.

The phase-set portion of the cycle uses the level-set signal information to achieve a particular remanent flux state which corresponds to the desired insertion phase level for the phase shifter. Setting of the remanent flux state can be done by direct open-loop construction of a driving pulse from the level-set signal or by a feedback arrangement in which information about the voltage amplitude and duration of an applied pulse is accumulated, compared with the level-set signal, and used to terminate the drive at the appropriate time. The simplest relationship of either type is one in which the Volt-time integral of the driving pulse is made to be proportional to the desired phase shift angle. In practice, it is necessary to calibrate the Volt-time integral to fit the actual phase shifter characteristics, and even to change this calibration as a function of operating frequency and temperature.

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2. Phase Shifter Control Characteristics

A typical control characteristic of a latching phase shifter and its electronic driver is shown in Fig. 2. The control characteristic will vary from phase shifter to phase shifter. Also, changing the r-f frequency or the ambient temperature will cause changes in the control characteristic. In order to accurately set the phase shifter, calibration curves for each device at various operating frequencies and temperatures are measured and stored either in the beam steering computer or in PROM at the driver itself. Errors of the order of three degrees rms are achievable for a 7-bit device over a ten percent frequency range and a temperature range of 90 degrees Celsius.
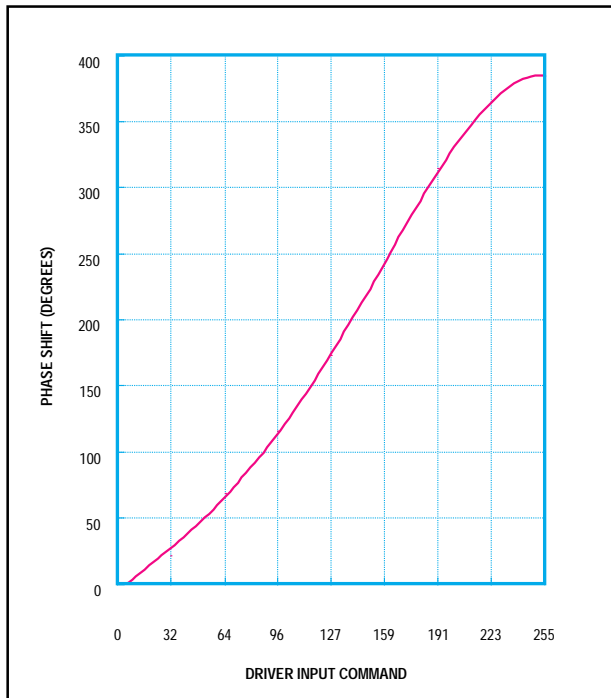

Figure 2. *Control Characteristic of a Latching Phase Shifter.*

3.1 MAG Driver Developments

For the past few years, MAG has been investigating methods of reducing driver cost. Removal of the requirements to mount the driver directly to the phase shifter has allowed us to bundle several drivers into one hybrid package with the very desirable effect of reducing both cost, size and weight.

To accurately establish to state of a ferrite phase shifter, the magnetic flux in the microwave ferrite

is set by measuring the volt-time product associated with the phase shifter SET pulse. Although the supply voltage is approximately constant, variations affect phase shifter performance unless compensation is provided. The MAG driver provides this compensation by sampling the phase shifter control voltage and digitally integrating the sampled voltage to provide accurate characterization of the volt-time product.

Using the digital integration described above, a new logic chip was developed using 5 Volt CMOS standard cells. The Application Specific Integrated Circuit (ASIC) chip provided the logic necessary to control four phase shifters. Built-in-test (BITE) was also incorporated into the driver to allow diagnostic testing of the driver and phase shifter. To prove the design, a breadboard was built using LSTTL logic. After verification of the design, the chip was physically realized in September 1988.

3.2 Driver Features

The driver provides the usual control waveforms for latching dual-mode ferrite phase shifters, e.g., a saturated reset pulse followed by a timed set pulse. The time of the set pulse is determined by the data word and the voltage applied to the phase shifter drive coils. The driver provides these waveforms for all channels simultaneously in the case of multichannel drivers.

Special features incorporated into the driver are:

> Built-in-test circuits which provide for the sensing of the set and reset currents in each channel and provide an indication of a failure.

> If a particular channel does not receive a new data word (parallel) or receives data word zero (serial), the output drivers are not activated during the switching cycle.

> Automatic shutdown of the driver limits the maximum set current, which protects the set output circuit if the phase shifter saturates.

The driver requires two power supplies. The first is the logic supply of 5 Volts which must be well regulated since this voltage is also the reference

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voltage for the A/D converter used in the ASIC to measure volt-time product. The supply must furnish 25 mA current to each ASIC connected to it. The second supply – which may have poor regulation – is the supply used to provide switching energy to the phase shifter. Since the phase shifter is a latching device, it only requires drive energy when it is desired to change the phase state. To reduce the peak current demands on the second power supply, local energy storage is provided by a capacitor located at the driver. Typically, the second power supply operates at 15 Volts. The current from this supply is dependent upon the geometry of the phase shifter being controlled and the switching rate of the phase shifter. The driver can be switched at rates up to 2 KHz.

The driver operates by sensing the reset current and turning off the voltage once the reset current has reached a given value – typically in the range 1.2 to 1.8 Amp. The set current is also sensed and the set circuit is protected by shutting off the driver whenever this current exceeds a predetermined limit. The threshold currents for the BITE circuits are 750 mA for the reset and 150 mA for the set.

Data is supplied to the driver via digital input signals. The logical low is between 0 and 1.5 Volts while the logical high is between 3.5 and 5.0 Volts. The input current in either the low or high state is less than or equal to 10 microamperes. Data may be entered using either a parallel or serial mode.

The parallel mode uses an 8-bit data bus and an address bus whose size is commensurate with the number of drivers connected to the data bus, i.e., a 4-bit address bus is sufficient to separately address 16 channels. Data on the data bus will be loaded to the address specified by the address bus upon the application of a signal to the data load (DL) line. The timing diagram is given in Fig. 3a. The maximum rate that data may be loaded is 5 MHz. The reset-set switching cycle is initiated by application of a signal to the output enable (OE) line.

The serial mode of operation requires the data to be entered into a latch on the driver via a clock signal. The maximum clock frequency is 5 MHz. The reset-set switching cycle may be initiated by the coincidence of the clock and the data or by a signal on an output enable (OE) line as shown in Fig. 3b.
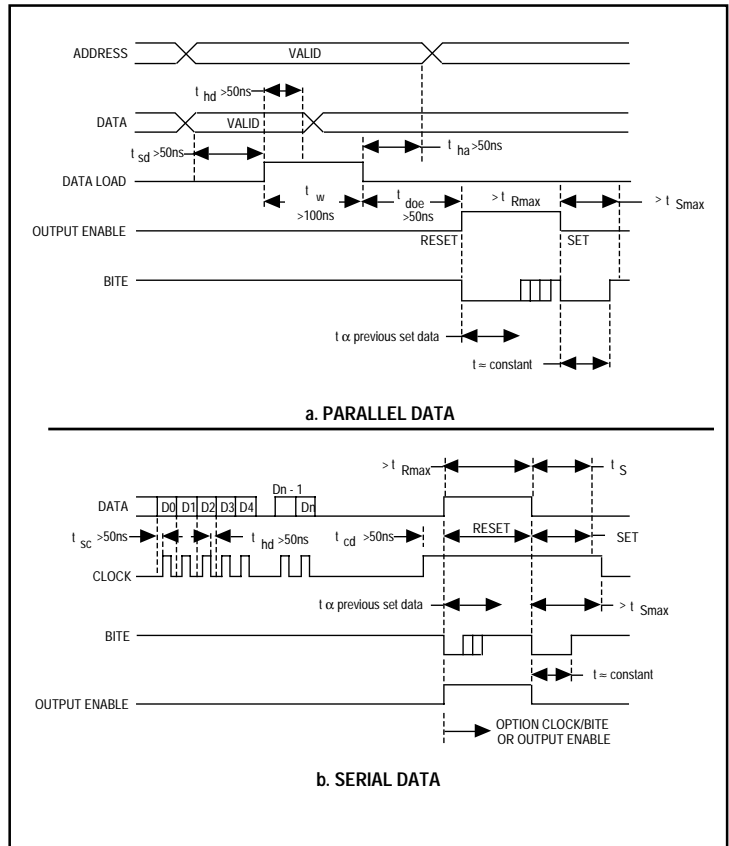

Figure 3. *Timing Diagrams.*

3.3 Driver Packaging

MAG has developed several techniques for packaging the logic chip and the associated power stages. The least costly of these uses discrete components mounted on a circuit board. The ASIC is mounted in a package which is hermetically sealed. Fig. 4 shows a realization of a four-channel driver which uses a parallel interface and Fig. 5 shows a four-channel driver using a serial interface. It is obvious that the serial interface results in a significant reduction in size at the cost of increased data loading time. What is not so obvious is the fact that the serial configuration results in increased reliability because of the fewer connections involved.

A phased array antenna will normally have a beam steering computer (BSC) which allows for temperature and frequency compensation required by the phase shifter. However, in some cases it is desirable to include memory on the driver to provide the necessary compensation. The single-channel driver shown in Fig. 6 uses discrete components and PROM storage to provide frequency and temperature compensation.

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The hybrid microelectronic circuit shown in Fig. 7 is a driver which controls eight phase shifters. Two ASICs as well as the crystals, resistors, capacitors and transistors are located on a substrate inside the hermetically sealed package. The size and weight reduction realized by this packaging technique is achieved with a significant cost penalty – particularly for small volume production.

A photograph of a driver containing 8 ASICs and capable of controlling 32 phase shifters is shown in Fig. 8. MAG has used this packaging extensively in phased arrays developed and delivered to the Naval Air Warfare Center at China Lake, California. The high density packaging results in the lowest possible costs.
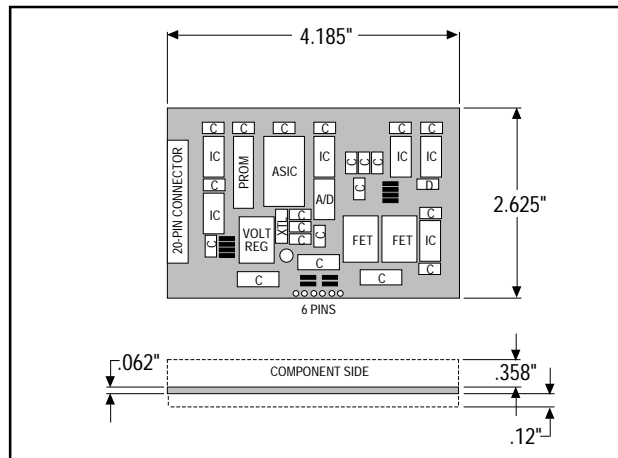

Figure 6. *Single-Channel Driver Incorporating a PROM for Frequency and Temperature Compensation.*
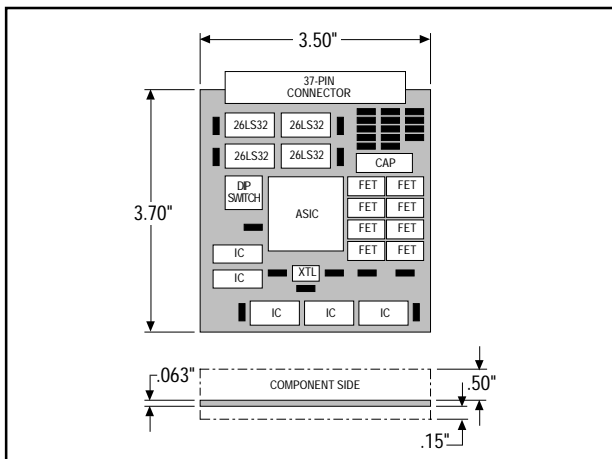

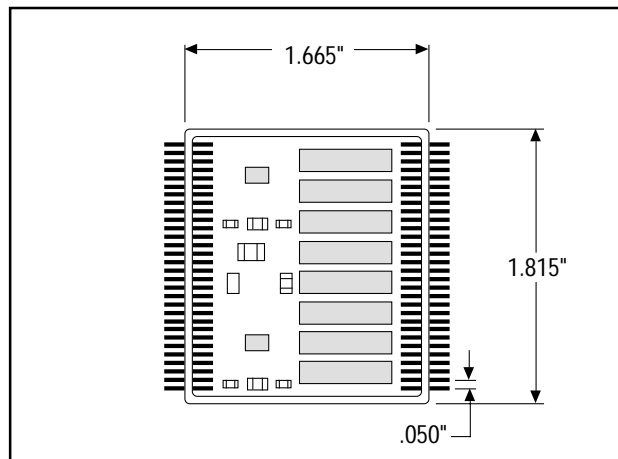**Figure 4.** *Four-Channel Driver, Parallel Mode.*
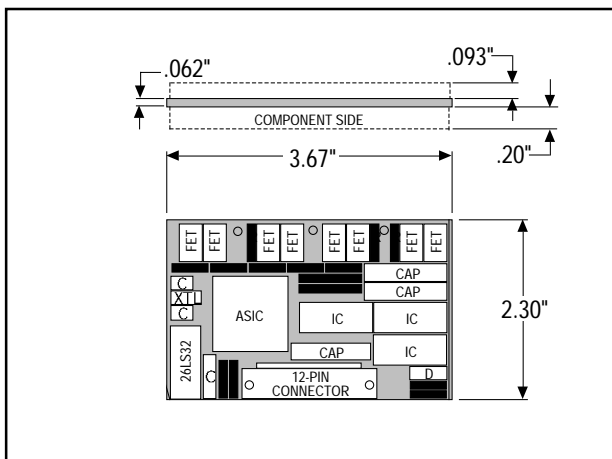

Figure 7. *Eight-Channel Driver Hybrid Package.*
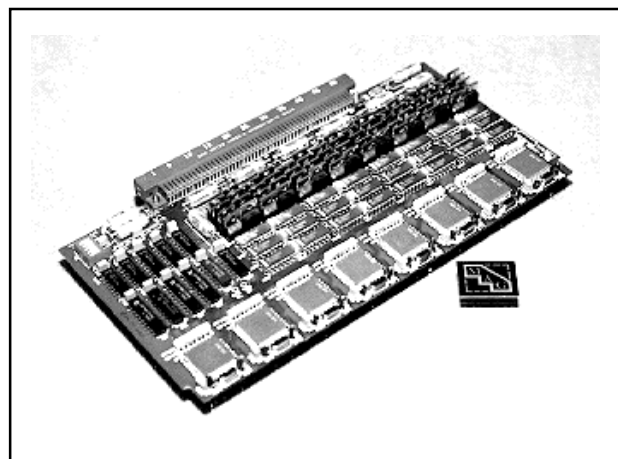

Figure 5. *Four-Channel Driver, Serial Mode.*

Figure 8. *Photograph of 32-Channel Driver Board.*